

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): An integrated circuit comprising:

scan chains implemented by registers disposed in a logic circuit, configured to shift in test patterns, to transfer the test patterns to the logic circuit, to receive test results of the logic circuit, and to shift out the test results;

a test pattern generation unit configured to transform the test patterns as scanning test patterns for feeding into the scan chains; and

a test result compression unit connected to the output stages of the scan chains, configured to compress the test results so as to generate the same number of compressed test result signatures as the number of the test results, ~~and to compare~~ transfer the resulting compressed test result signatures with ~~[[to]]~~ the scan chains in ~~a first~~ order to allow one-to-one mapping, and to detect the scan chain which fails to match the compressed test result signature corresponding to each scan chain.

Claim 2 (Currently Amended): The integrated circuit as claimed in claim 1, further comprising:

an expected value comparison circuit configured to compare the compressed test result signatures with a corresponding expected value in ~~the first~~ order, and detects a compressed test result signature which fails to match the corresponding expected value.

Claim 3 (Currently Amended): The integrated circuit as claimed in claim 2, further comprising:

a failure scan chain determination circuit configured to count the order of a compressed test result signature which fails to match the corresponding expected value

during comparison in ~~the first~~ order, and determines a failure scan chain, which includes a failure detected in the scan chains.

Claim 4 (Currently Amended): The integrated circuit as claimed in claim 1, wherein the test result compression unit includes:

data compression units connected to the respective output terminals of the scan chains, configured to receive the test results, and to transfer the compressed test result signatures, the number of the data compression units is the same as the number of the test results; and

a parallel to serial converter connected to all of the data compression units, configured to receive the compressed test result signatures in parallel, and to serially transfer the compressed test result signatures in ~~the first~~ order.

Claim 5 (Currently Amended): The integrated circuit as claimed in claim 1, wherein the test result compression unit comprises:

a ~~first~~ selector connected to the output terminals of the scan chains, configured to select and transfer the test results in ~~a second~~ order;

a plurality of data compression units connected to the first selector configured to receive the test results, and to transfer the compressed test result signatures, the number of the data compression units being smaller than the number of the test results; and

a parallel to serial converter connected to the data compression unit configured to receive the compressed test result signatures in parallel, and to serially transfer the compressed test result signatures in ~~the first~~ order.

Claim 6 (Currently Amended): The integrated circuit as claimed in claim 1, wherein the test result compression unit comprises:

a mode changeover circuit connected to the output stages of the scan chains configured to receive the test results in parallel and output the test results in parallel in a self-test mode, to receive the test results in parallel in a failure analysis mode, and to transfer the test results to the scan chains in a ~~first~~ order that allows one-to-one mapping; and

a data compression unit connected to the mode changeover circuit configured to receive the test results in parallel in the self-test mode, to collectively compress ~~compresses~~ the test results into a single compressed test result signature, and to compress ~~compresses~~ the test results in ~~the first~~ order in the failure analysis mode.

Claim 7 (Currently Amended): The integrated circuit as claimed in claim 1, wherein the test pattern generation unit divides the test pattern, generating scanning test patterns;

the scan chains shift in the scanning test patterns and simultaneously ~~simultaneously~~ transfer the scanning test patterns to the logic circuit, receive the test results from ~~from~~ the logic circuit, and shift out ~~the~~ block test results dividing the test results from respective last stages of blocks in the scan chains; and

the integrated circuit further comprises a block compression unit configured to receive the block test results, to compress the test results so as to generate the same number of compressed test result signatures as the test results, and to transfer the resulting compressed block test result signatures to the blocks in a ~~third~~ order that allows one-to-one mapping.

Claim 8 (Currently Amended): The integrated circuit as claimed in claim 7, further comprising:

a block expected value comparison circuit configured to compare the compressed block test result signatures with the corresponding expected values in ~~a third~~ order, and to detect a compressed block test result signature that fails to match the corresponding expected value; and

a failure block determination circuit configured to count the order of the compressed block test result signature that fails to match the corresponding expected value in ~~the third~~ order, and to identify a failure block having a failure detected in the blocks.

Claim 9 (Currently Amended): The integrated circuit as claimed in claim 7, wherein the block compression unit comprises:

~~second~~ data compression units, connected to the output terminals of the blocks, configured to receive the block test results, and to transfer compressed block test result signatures, the number of the ~~second~~ data compression units is the same as the number of the block test results; and

a ~~second~~ parallel to serial converter configured to receive in parallel the compressed block test result signature from the ~~second~~ data compression units, which are connected to the divided blocks in one of the scan chains, and to serially transfer the compressed block test result signatures in ~~the third~~ order.

Claim 10 (Currently Amended): The integrated circuit as claimed in claim 7, wherein the block compression unit comprises:

a ~~second~~ selector configured to transfer the block test results delivered from a failure scan chain; and

~~second~~ data compression units connected to the ~~second~~ selector, configured to receive the block test results, and to transfer the compressed block test result signatures, the number of the ~~second~~ data compression units is smaller than the number of the block test results; and

a ~~second~~ parallel to serial converter configured to receive in parallel the compressed block test result signatures from the ~~second~~ data compression unit connected to the divided blocks in one of the scan chains and to serially output the compressed block test result signatures in ~~the third~~ order.

Claim 11 (Currently Amended): The integrated circuit as claimed in claim 7, wherein the block compression unit comprises:

a ~~second~~ selector connected to output terminals of the blocks, configured to select and to transfer each of the block test results in a ~~fourth~~ order; and

data compression units connected to the ~~second~~ selector, configured to receive the block test results and to transfer the compressed block test result signatures, the number of the data compression units is smaller than the number of the block test results.

Claim 12 (Currently Amended): The integrated circuit as claimed in claim 3, wherein the test pattern generation unit is initialized as the test pattern into scanning test patterns in a failure pattern determination mode, a failure shift register determination mode, and a failure block determination mode;

the scan chains shift in the scanning test patterns, simultaneously transfer the scanning test patterns to the logic circuit, and receive the test results from the logic circuit, and in the failure pattern determination mode and the failure shift register determination mode, shift out the test results from the last stages of the scan chains, and in the failure block determination

mode, shift out the block test results, which result from dividing the test results, from the last stages of ~~the~~ divided blocks in the scan chains; and

the test result compression unit receives the test results in parallel and collectively compresses the test results into a single compressed test result signature in the failure pattern determination mode, and in the failure shift register determination mode, transfers the compressed test result signature in ~~the first~~ order, and in the failure block determination mode, receives the block test results, compresses the test results so as to generate the same number of compressed test result signatures as the test results, and transfers the resulting compressed block test result signatures to the blocks in ~~a third~~ order that allows one-to-one mapping.

Claim 13 (Currently Amended): The integrated circuit as claimed in claim 12, wherein the test result compression unit comprises:

a ~~second~~ selector configured to transfer the test results in the failure pattern determination mode and the failure shift register determination mode, and in the failure block determination mode, to select and to transfer the block test results in ~~a fourth~~ order;

a mode changeover circuit connected to the ~~second~~ selector, configured to receive and to transfer the test results in parallel in the failure pattern determination mode, to receive the test results in parallel and to transfer the test results in parallel in ~~the first~~ order in ~~the~~ a failure scan chain determination mode, and to transfer the block test results output from the failure scan chain in the failure block determination mode; and

a data compression unit connected to the mode changeover circuit, configured to receive the test results in parallel and to collectively compress, the test results into a single compressed test result signature in the failure pattern determination mode, to compress each of the test results in ~~the first~~ order and to transfer the resulting compressed test result

signature ~~in the first order~~ in the failure scan chain determination mode, and to compress each of the block test results ~~in the third order~~ and to transfer the resulting compressed block test results ~~in the third order~~ in the failure block determination mode.

Claim 14 (Currently Amended): The integrated circuit as claimed in claim 7, wherein the block compression unit comprises:

an exclusive-OR calculation unit configured to transfer an exclusive-ORed value of the block test results, which are delivered from the scan chains including a failure scan chain;

~~second~~ data compression units connected to the exclusive-OR calculation unit, configured to receive the exclusive-ORed value, and to transfer the compressed block test result signatures, the number of the ~~second~~ data compression units is smaller than the number of the block test results; and

a ~~second~~ parallel to serial converter configured to receive in parallel the compressed block test result signatures from the ~~second~~ data compression unit connected to the divided blocks in one of the scan chains and to serially transfer the compressed block test result signatures in ~~the third~~ order.

Claim 15 (Currently Amended): The integrated circuit as claimed in claim 7, further comprising:

a register selection circuit configured to select each of the registers implementing the blocks in ~~a fourth~~ order; and

a register inversion circuit configured to ~~configured to~~ invert one of the value of the block test result and the value of the block test pattern received by a selected one of the registers into the resulting inverted block test result, the block compression unit receives the

inverted block test result and compresses the inverted block test results into the resulting compressed, inverted block test results.

Claim 16 (Currently Amended): The integrated circuit as claimed in claim 15, wherein ~~the~~ a block expected value comparison circuit compares the compressed, inverted block test results with ~~the~~ corresponding expected values, and detects a compressed, inverted block test result that matches that corresponding expected value; and

the integrated circuit further comprises a failure register determination circuit configured to count the order of the compressed, inverted block test result that matches the corresponding expected value in ~~the fourth~~ order, and to identify a failure register having a failure detected in the blocks.

Claim 17 (Currently Amended): The integrated circuit as claimed in claim 15, wherein

the register selection circuit comprises a first shift counter which selects each of the registers in ~~the fourth~~ order; and

the register inversion circuit comprises a toggle F/F circuit configured to control a hold/inversion of one of the value of the block test result and the value of the block test pattern received by a selected one of the registers.

Claim 18 (Original): The integrated circuit as claimed in claim 15, wherein at least two registers influenced by a failure belong to different scan chains.

Claim 19 (Withdrawn): A computer implemented apparatus for designing an integrated circuit comprising:

a net list generation unit configured to generate a net list for



a test pattern generation unit configured to divide a test pattern into a plurality of scanning test patterns,

scan chains implemented by registers disposed in a logic circuit, configured to shift in the scanning test patterns and to simultaneously transfer the scanning test patterns, and to receive test results from the logic circuit and to shift out the test results, the number of the scan chains is the same as the number of those test results, and

a test result compression unit connected to the output stages of the scan chains to compress the test results so as to generate the same number of compressed test result signatures as the test results, and to transfer a resulting compressed test result signatures to the scan chains in a first order that allows one-to-one mapping; and

a self-test circuit insertion unit configured to insert the net list for the test pattern generation unit, the scan chains, and the test result compression unit in the net list for the integrated circuit.

Claim 20 (Withdrawn - Currently Amended): A computer implemented apparatus for designing scan chains implemented by registers in an integrated circuit comprising:

a logical cone extraction unit ~~configured~~ configured to extract a logic circuit that outputs a value according to changeable input values in the registers, and to generate a logical cone, which is a combination circuit that is included by the logic circuit, for each register;

a dependency extraction unit configured to generate a group of the registers in the logical cone including the same logic circuit; and

a scan chain configuration unit configured to generate any scan chains using only the registers not belonging to the same group.